

CPT-DATS
CPT-DA2810 Interface Card
Technical Brief

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Card Version 1.1

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CPT-DATS Manual Revision History

CARD VERSION 1.0: Initial Board for test only purposes.

CARD VERSION 1.1: Modified to include generic I/O and standard header interfaces.

Release 1.0 – Initial Release

Release 1.1 – Minor typographical corrections

Release 1.2 – Modified default link settings for Communications Ports

CARD VERSION 1.2: Minor Board modifications – not released as at 27/06/08

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CPT-DATS INTERFACE BOARD TECHNICAL BRIEF

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1.0 Overview of the CPT-DATS Interface Board

The CPT-DATS is an interface board designed to provide an easy and flexible development environment for the CPT-DA2810 (TMS320F2810 DSP) controller board. The CPT-DATS board has a DSP Controller Interface (compatible with the CPT-DA2810) and provides an on-card regulated power supply, non-isolated RS-232 serial communications and 3.3V to TTL level translation interfaces.

The board is intended to simplify program development for the CPT-DA2810 platform.

In addition, the CPT-DATS board can be configured to provide a fully automatic test environment for the CPT-DA2810 circuit board.

The CPT-DATS measures 173 x 86mm.

Please consult the CPT-DA2810 Technical Manual for a detailed description of the functionality of the CPT-DA2810 processor card.

The CPT-DATS board provides buffering and signal conditioning for digital signals to the DSP Controller Interface. This includes level-shifting of the digital I/O between the DSP Controller Interface 3.3V and the external TTL level (5V). All analog signals are passed directly through to the DSP Controller Interface.

The CPT-DATS board requires a CPT-DA2810, or equivalent, DSP processor card to operate.

The basic functionality of the CPT-DATS is:

- 16 off buffered complementary TTL-level gate driver PWM outputs, with common fault interrupt and enable (also able to be configured as Digital Outputs)
- 8 off TTL-level individually configurable digital I/O bits, with common interrupt
- 7 off TTL-level interrupt and capture port inputs
- 2 banks of 6 off 12-bit 0-3V ADC inputs
- 2 off output LEDs
- 2 off non-isolated RS-232 level serial communications port
- 12V Power Supply Input
- On-card voltage regulation
- 80-way DSP Controller Interface plug-in connector (compatible with CPT-DA2810)
- Reset push button

Figure 1-1 shows a functional block diagram of the CPT-DATS card, illustrating all major sections.

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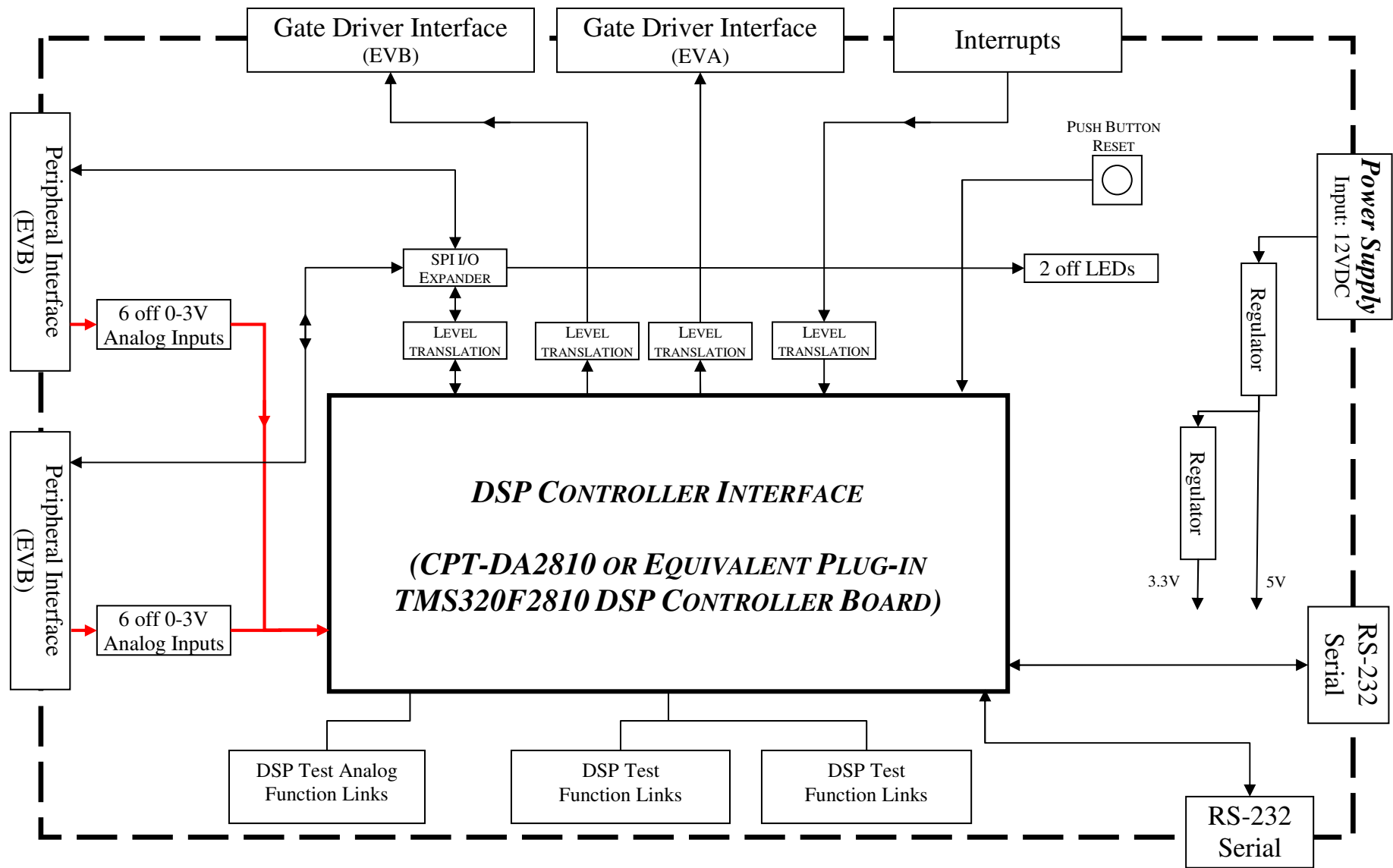


Figure 1-1: Functional Diagram of CPT-DATS Interface Board

1.1 Digital I/O

The CPT-DATS interface board supports up to 33 bits of digital I/O, consisting of 7 digital inputs, 16 bits of buffered TTL level digital outputs, 2 on-card LED outputs and 8 bits of buffered TTL level digital I/O. All digital I/O bits are fully buffered with level shifts between 3.3V and 5V TTL levels where necessary.

The 7 off digital inputs are all buffered and feed directly to the DSP Controller Interface. They are assigned to pins on the Interface that can be configured to trigger interrupts or capture ports.

The 8 bits of buffered TTL level digital I/O can be individually configured as either inputs or outputs via the SPI available on the DSP Controller Interface. They are separated into 2 banks of 4-bits and they can be individually set to trigger a common on-card interrupt.

The CPT-DATS interface card supports a maximum of 16 bits of buffered digital outputs that are configured as two banks of 8 fed directly from the DSP Controller Interface (assigned to pins shared with the Event Manager A and B PWM) and two on card LEDs that are also driven via the SPI.

The header files for the DSP controller board will select the default modes of operation for all of the pins on the board. The user is advised to refer to this file, *cpt-dats.h* before programming of any software code.

1.2 Analog Inputs

The CPT-DATS interface board has 12 off analog inputs configured as 2 banks of 6 0-3V ADC signals (ADCINA0-A5, ADCINB0-B5). Each bank is available on a separate IDC header and is passed directly to the DSP Controller Interface with no on-card buffering, filtering, or protection. The CPT-DA2810 DSP Controller board has on-card glitch filters and over-voltage protection diodes.

Please consult either the *CPT-DA2810 Technical Manual* or the Texas Instruments documentation on the ADC converter for further information. *TMS320x281x DSP Analog-to-Digital Converter (ADC) Reference Guide*, Literature Number: *SPRU060D*

The CPT-DA2810 contains precision reference inputs for self calibration of the analog inputs. It is strongly recommended that the ADC be software calibrated for both gain and offset.

A 2.5V buffered reference is available on each of the analog IDC headers for use off card. This reference is generated from the 2.5V reference signal that is supplied to the DSP Controller Interface by the plug-in controller board.

1.3 Gate Drive Interface

The CPT-DATS is configured with two off 26-way headers, each of which contains 8 off TTL level PWM channel outputs. The PWM signals are sourced from the DSP Controller Interface and fed through a level shift to produce the TTL level outputs.

Each group of 8 PWM output is assigned to pins on the DSP Controller Interface that correspond to a single Event Manager. The Gate Drive Interface also contains a gate fault signal that is fed to the corresponding PDPINT* pin on the DSP Connector Interface and a gate reset signal that can initiate a system reset in the event of a fault.

The card has pull-down resistors on the PWM outputs to ensure that they are left in a normally low state if fault is triggered.

1.4 Communications

The CPT-DATS interface board supports two off non-isolated RS-232 serial communications port that interfaces the plug-in DSP controller to a PC terminal emulation program to aid in program development.

1.5 Power Supply

The standard CPT-DATS interface card operates from a nominal +12VDC. The board has an on-card SMPS that generates regulated +5V and +3.3V supply.

The board should not be powered without an appropriate plug-in DSP Controller connected to the DSP Controller Interface

2.0 Specifications

2.1 DSP Controller Interface

Configuration	80-way IDC Header compatible with the CPT-DA2810, or equivalent processor Please consult the <i>CPT-DA2810 Technical Manual</i> for the Technical Specifications of this board.
Power Supply	Analog Supply: 5V (DSP Controller Interface Pin 58) AGND (DSP Controller Interface Pins 63, 66, 69, 72, 75, 78, 80)
	Digital Supply: 3.3V LED (DSP Controller Interface Pins pin 7) GND (DSP Controller Interface Pins 4-6)
PCB Connection	80-way plug-in header (X5)

2.2 Analog Inputs

2.2.1 AC General Inputs

Definition	12 off 0-3V analog inputs with no on-card filtering ADCINA0-5 ADCINB0-5 Note: The CPT-DA2810 contains a low pass or “glitch” filter and a diode clamp circuit
Input Voltage Range	0-3V maximum
Dynamic Response	Cut-off frequency >150kHz
PCB Connections	ADCINA0-5 on 26-way IDC header (X7) ADCINB0-5 on 26-way IDC header (X4)
DSP Controller Interface	Pins 60-80

2.3 Digital I/O

Definition	8 bits of individually configurable Digital I/O Expansion Port 0x00 addressable through the SPI Interface
Digital high input voltage threshold	4.0V
Digital low input voltage threshold	1.0V
Interrupt Capable	Yes, Common Digital Interrupt Input to CAP3 on the DSP Controller Interface.
Digital I/O rated at	Source 3mA per bit, ABSOLUTE MAXIMUM. Sink 8mA per bit, ABSOLUTE MAXIMUM.
PCB Connection	DIGIOA4-7 – 16-way IDC header (X4) DIGIOA0-3 – 16-way IDC header (X7)
DSP Controller Interface	Accessed via the SPI Interface Pins 14 (SPISIMO), 15 (SPISOMI), 16 (SPICLK) and 17 (SPISTE*)

2.4 Digital Inputs

2.4.1 Interrupt Capable Digital Inputs

Definition	7 bits total 2 off PDPINT* Gate Driver Interrupt Inputs (PDPINTA*, PDPINTB*) 3 off TTL-level External Interrupt Inputs (XNMI, XINT2, XINT1) 2 off TTL-level Capture Port Inputs (CAP1, CAP4) Note: Digital I/O Expansion Port 0x00 can be configured to be interrupt driven providing 8 additional indirect interrupt driven inputs.
Digital high input voltage threshold	3.85V
Digital low input voltage threshold	1.65V
Digital Input rated at	Sink 24mA per bit, ABSOLUTE MAXIMUM
PCB Connection	PDPINTA* (G_FAULTA*) – 26-way IDC header (X2) & 16-way IDC header (X3) PDPINTB* (G_FAULTB*) – 26-way IDC header (X1) & 16-way IDC header (X3) XNMI (5VXNMI), XINT2 (5VXINT2), XINT1 (5VXINT1), CAP1 (5VCAP1), CAP4 (5VCAP4) – 16-way IDC header (X3)
DSP Controller Interface	Pins 18-20, 23, 31, 41, 49

2.5 PWM Gate Drive Interface - EVA

Definition	1 off 8 PWM Outputs within Event Manager A Also able to be configured as Digital Outputs
PWM Outputs per Event Manager	Event manager has 8 PWM outputs consisting of – 3 independent complementary pairs (6 outputs) with programmable deadband generation 2 gate drive outputs generated from two independent outputs, for which deadband compensation must be implemented in software
Gate Fault Interrupt	PDPINTA*, which when unmasked and activated, immediately disables the PWM outputs. Response time is ~12nsec after fault detection The PWM signals are placed into a high impedance state and have on-card pull-down resistors
Output rated at	±24mA per bit, ABSOLUTE MAXIMUM
Gate Reset	Normally Low Gate Reset Signal
Output Voltage	0-5V
PCB Connections	26-way IDC header (X2)
DSP Controller Interface	Pins 22, 23, 32-39

2.6 PWM Gate Drive Interface - EVB

Definition	1 off 8 PWM Outputs within Event Manager B Also able to be configured as Digital Outputs
PWM Outputs per Event Manager	Event manager has 8 PWM outputs consisting of – 3 independent complementary pairs (6 outputs) with programmable deadband generation 2 gate drive outputs generated from two independent outputs, for which deadband compensation must be implemented in software
Gate Fault Interrupt	PDPINTB*, which when unmasked and activated, immediately disables the PWM outputs. Response time is ~12nsec after fault detection The PWM signals are placed into a high impedance state and have on-card pull-down resistors
Output rated at	±24mA per bit, ABSOLUTE MAXIMUM
Gate Reset	Normally Low Gate Reset Signal
Output Voltage	0-5V
PCB Connections	26-way IDC header (X1)
DSP Controller Interface	Pins 40, 41, 50-57

2.7 Communications Interface

2.7.1 RS-232 Interface

Definition	RS-232 connection, providing two pin serial communications for interface to a standard PC serial port from SCIA on the DSP Controller Interface
Compatibility	Links provided to enable the board to be configured as a DTE or a DCE (LK3). Default is configuration as a DCE
PCB Connections	10-way IDC connector, with pin outs to suit standard PC 9 pin serial port (X8)
DSP Controller Interface	Pins 10, 11 (SCIA)

Definition	RS-232 connection, providing two pin serial communications for interface to a standard PC serial port from SCIB on the DSP Controller Interface
Compatibility	Links provided to enable the board to be configured as a DTE or a DCE (LK4). Default is configuration as a DCE
PCB Connections	10-way IDC connector, with pin outs to suit standard PC 9 pin serial port (X43)
DSP Controller Interface	Pins 12, 13 (SCIB)

2.7.2 Serial Peripheral Interface – SPI

Definition	<p>Four-pin serial peripheral interface (SPI) made available from the DSP Controller Interface</p> <p>It is a high speed, synchronous serial I/O port that allows a serial bit stream of programmed length (one to sixteen bits) to be shifted into and out of the device at a programmable bit-transfer rate</p> <p>Used to drive the on-card SPI to Digital I/O Expansion Chip</p>
Compatibility	4 wire SPI mode
DSP Controller Interface	Pins 14 (SPISIMO), 15 (SPISOMI), 16 (SPICLK) and 17 (SPISTE*)

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2.8 General

Physical Dimensions	L: 86mm
	W: 173mm
	H: \approx 27mm
Mounting Arrangement	4 off 3.5 mm holes 78mm x 165mm apart, located in the corners of the board
Environmental	-40 – 85°C ambient operating temperature 5% - 95% non condensing humidity

2.9 Power Supply

Input Voltage Range	12VDC
Standalone Input Current	100-250mA (depending on the active sections within the DSP)
Max Input Power	Approx. TBD ~500mW
Supplies Generated on-card	+5V Digital
	+3.3V Digital
	+2.86V Analog On-card Buffered Reference
	+2.5V Analog Buffered Reference
Input Power Connector	2-way IDC Connector (X6)

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Appendix

Appendix A Component Layout

Top Layer

